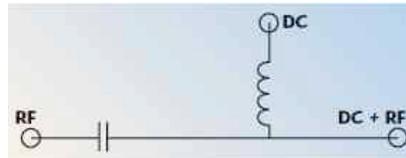


Wideband Bias Tee

Gary W. Johnson, WB9JPS

11-8-08

Bias tees are useful for injecting DC bias to a device under test while isolating an instrument from any DC offset. For instance, you may be applying a bias to the base of a transistor while using a network analyzer to measure S parameters. Or, when testing a modulated laser diode, a DC operating current is required while an ac modulation rides on top of that.



Conceptually, the simplest bias tee is just a coupling capacitor and an inductor, and is in effect a diplexer. For real-world components, the big shortcoming is inductor performance, especially self-resonance. If you are only interested in a narrow band of frequencies (say, one decade), the solution is indeed a simple LC network, and is no different than an RF choke and coupling capacitor on the output of an RF amplifier. But wideband applications—covering multiple decades in frequency—are more difficult and this is the performance we seek for test and measurement applications.

One solution is to design a series of damped lowpass filter sections where each inductor is only required to operate over a little more than one decade of frequency. Damping is very important and requires experimentation. With no damping, return loss and isolation exhibit large undesired deviations at many frequencies as you'll see later. A side effect of those large deviations is poor time domain response. If you want to use your bias tee to transmit fast digital pulses, you need to achieve smooth frequency-domain behavior, which typically translates into good pulse fidelity. Such a design should be good enough for TDR work.

Main specifications for a bias tee are:

Insertion loss (S_{21}): Ideally, it looks like a capacitor between the RF and RF+DC connectors.

Crossover frequency: The -3dB point on insertion loss.

Bandwidth: Maximum usable RF frequency.

Return loss (S_{11}): Again, a perfect bias tee looks like a capacitor and return loss is very low once you get above the crossover frequency.

Isolation: Attenuation of RF signals at the DC bias port. Typically you can expect $>25\text{ dB}$ if the bias source has a 50 ohm impedance, and much more if its impedance is lower, such as that of a power supply.

Current: Maximum DC current rating. Isolation, and sometimes return loss, suffer when inductors saturate.

The primary specs I was shooting for are:

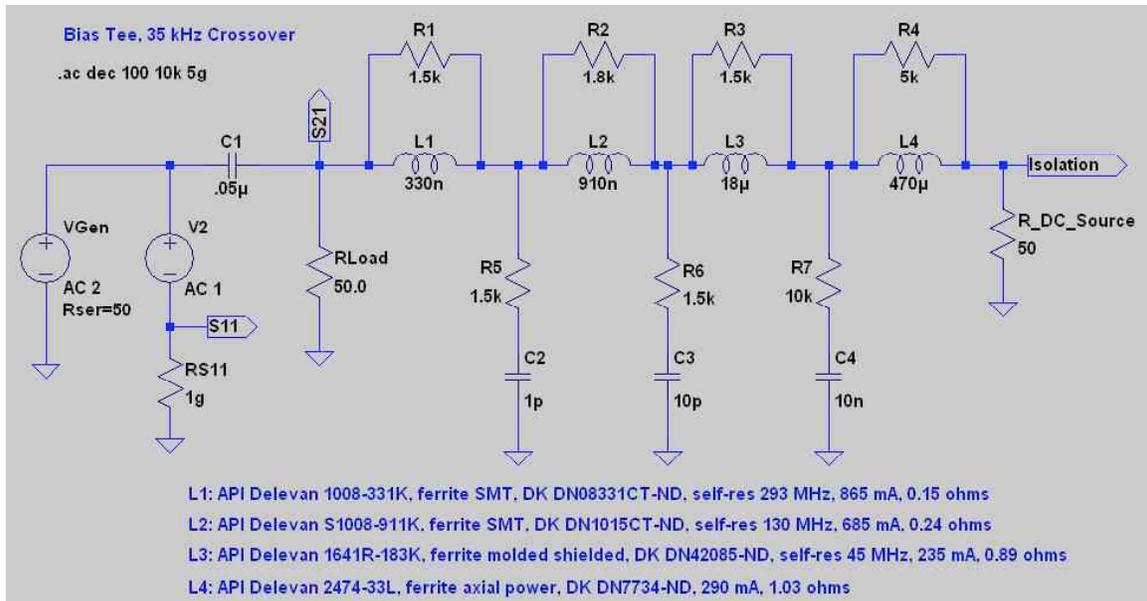
- Bandwidth 50 kHz to ~1 GHz
- Current 250 mA
- Return loss 30 dB
- Clean edges on fast pulses, <5% overshoot

My design topology is stolen from a Picosecond Pulse Labs 5546, which I had on hand at work and attempted to reverse-engineer. All of their bias tees use this same topology, adding or subtracting sections depending upon desired bandwidth. Their designs are among the few on the market that are fully qualified for clean time domain response. I once tested a general-purpose Mini-Circuits RF bias tee, running 1.2 GHz communications pulses through it, and it was pretty much a disaster with a great deal of overshoot and ringing. But it still works fairly well for sinusoidal steady-state applications. All of these bias tees are fairly expensive, several hundred dollars even on the surplus market.

To my knowledge, there are no formulae or formal approaches published for broadband bias tee design. Basic rules give us only a starting point. First, the cutoff frequency for the capacitor is given by $f_c = 1/(2\pi RC)$ where R is 100 ohms because the source and load are effectively in series. Next, the inductor's cutoff frequency should be lower than that of the capacitor and is computed by $f_l = R/(2\pi L)$ where R is again 100 ohms, assuming that the DC port is terminated in 50 ohms. Note that using a lower termination value on that port, such as a DC power supply, serves to lower the cutoff frequency even more, which is fine.

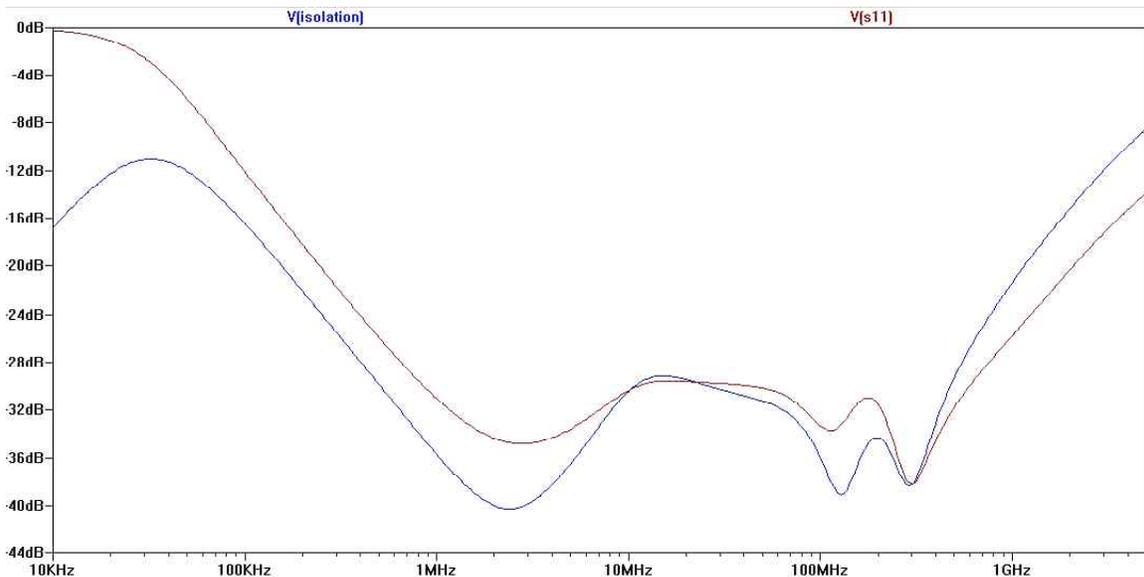
After some experimentation in LT-Spice, the circuit shown below has values that seem appropriate for high-frequency extension near 1 GHz. Each inductor has parasitic series resistance and parallel capacitance from the datasheet included in the model. I guessed at values for parasitic capacitance on L4. The technique for extracting S parameters comes from a W7ZOI article.¹

¹ Wes Hayward, *Scattering Parameter Extraction in SPICE*, <http://w7zoi.net/S-param%20extraction.pdf>

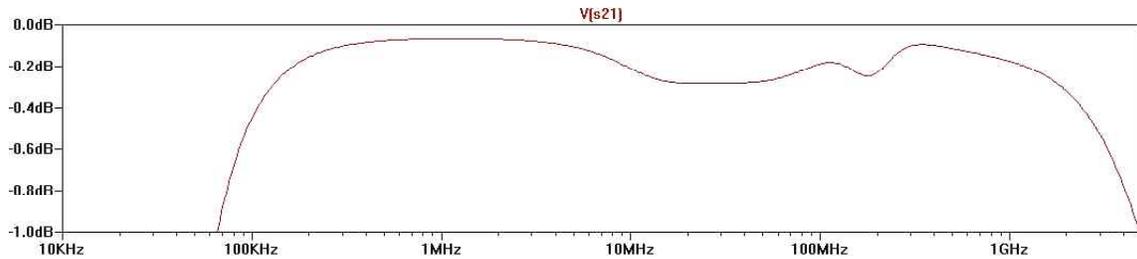


The graph below shows return loss and isolation. Return loss is better than 27 dB (SWR <1.09:1) from 550 kHz to 800 MHz. Isolation (with a 50 ohm DC source) is nearly as good. If driven by a zero-resistance power supply, isolation increases to >50 dB. You should be able to run 250 mA through this with only modest degradation in isolation, and no heating problems.

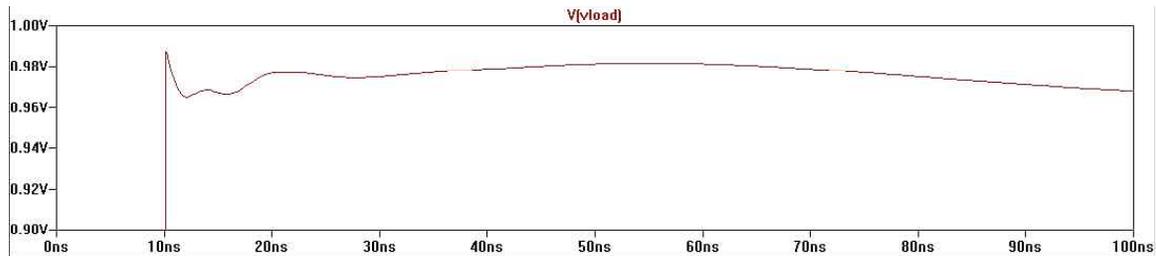
For more high-frequency extension, L1 could be changed to a smaller value, but it needs a very high self-resonant frequency, such as a Pulse Engineering PE-0805CM820JTT (82 nF, 0805, $f_s = 1.3$ GHz). A simulation indicated that return loss was 24 dB out to 3.5 GHz. Of course, this is just a simulation and layout effects will surely dominate. This being a simple amateur implementation, I have little faith in those predictions.



Insertion loss is less than 0.3 dB above the crossover frequency with low ripple. I spent a fair amount of time experimenting with damping values and various inductors, but was unable to improve overall performance beyond what is shown here.

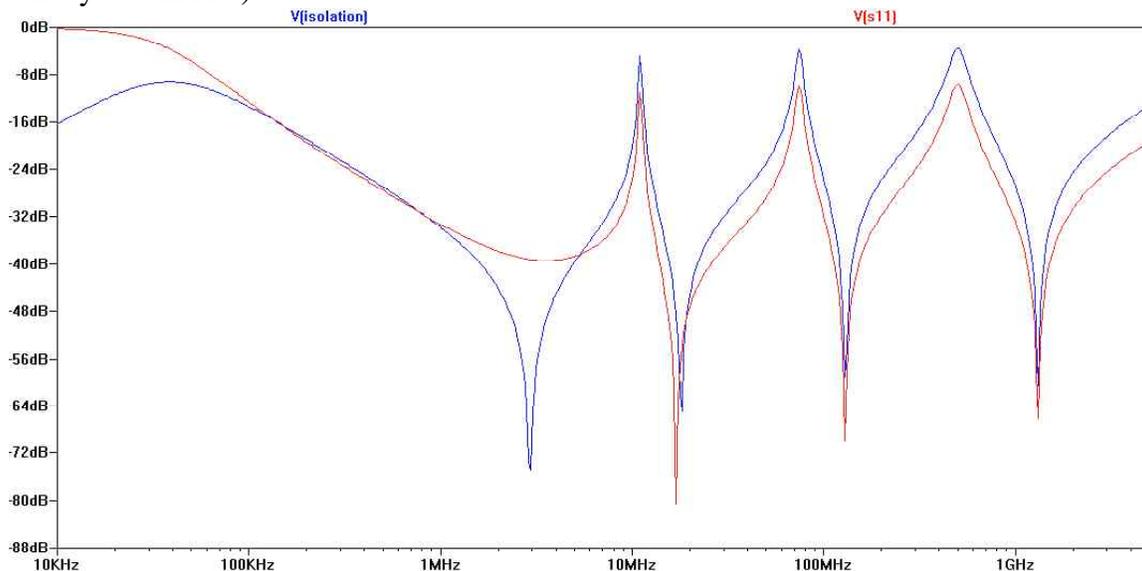


For the time domain response, I did a transient analysis in LTSpice. In this case, the input was a pulse starting at $t=10$ ns with a 100 ps risetime. Ideally, you would see a square edge settling at 1.00 V. The network's small loss is apparent, as is the short-term transient aberration amounting to about 2% of amplitude. If the actual circuit works this well, it could be useful for TDR measurements and digital signals to the 1 ns domain.

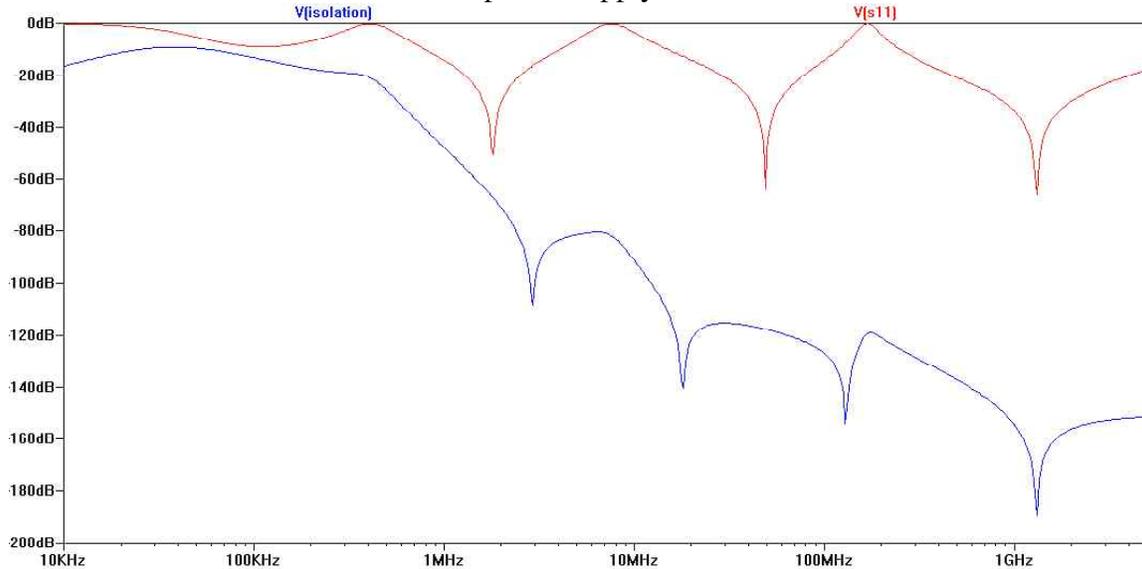


Some Defective Designs

Just for fun, let's look at some extreme designs. Here's what happens if you have nothing but inductors (this version had slightly different values for L1 and L2, but is typical of what you will see.)

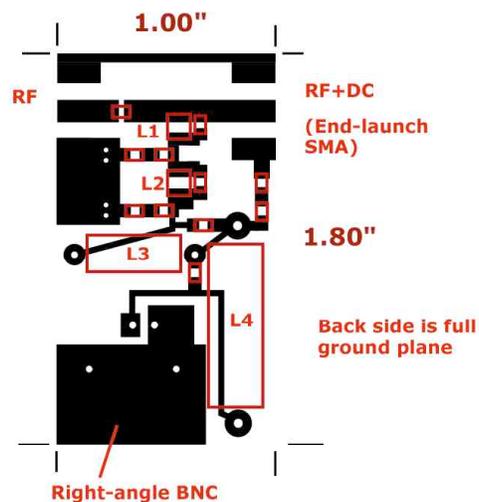


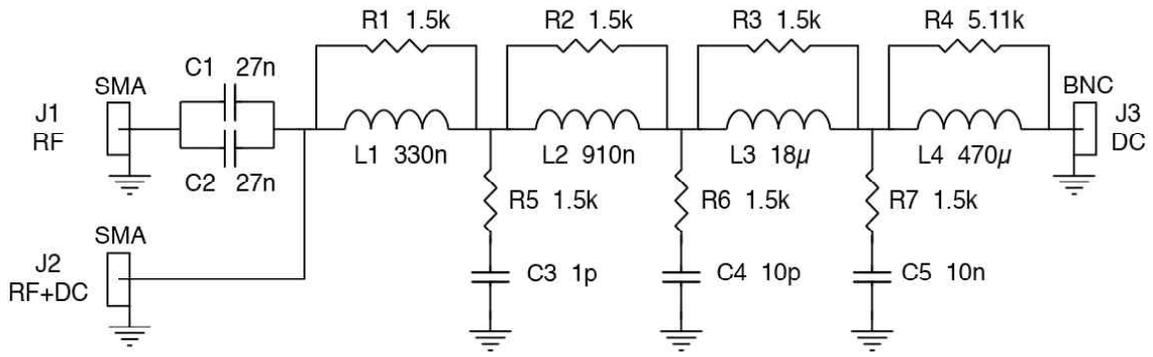
And here's what happens if you have just inductors and bypass caps: great isolation, but awful return loss. This is more like a power supply filter than a bias tee.



The Build

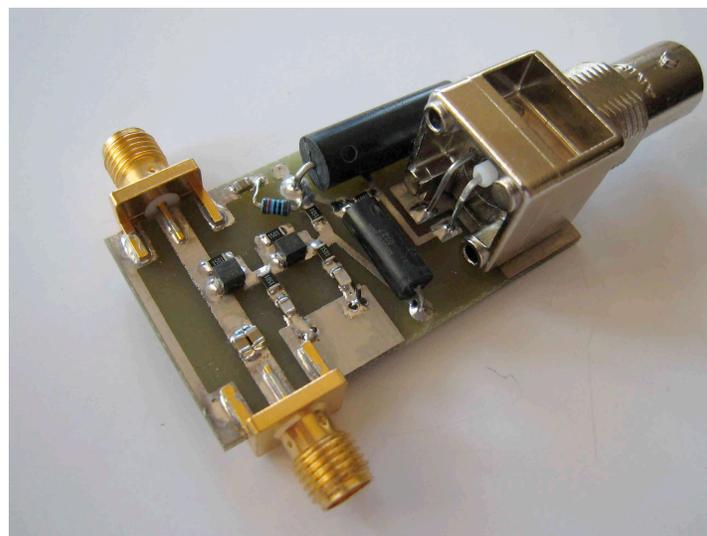
I laid out a board and fabricated several by using a toner transfer film (Techniks Press-N-Peel), then finished with electroless tin plating. The back is a full ground plane. All parts were SMT except L3 and L4, and one resistor (R7). The main coupling capacitor C1 was a pair of 27 nF 0805 parts in parallel. RF connectors are end-launch SMAs and the DC connector was a right-angle BNC. All parts were mounted on the top side to minimize overall thickness and make it easier to install a soldered-up shield when testing is complete.





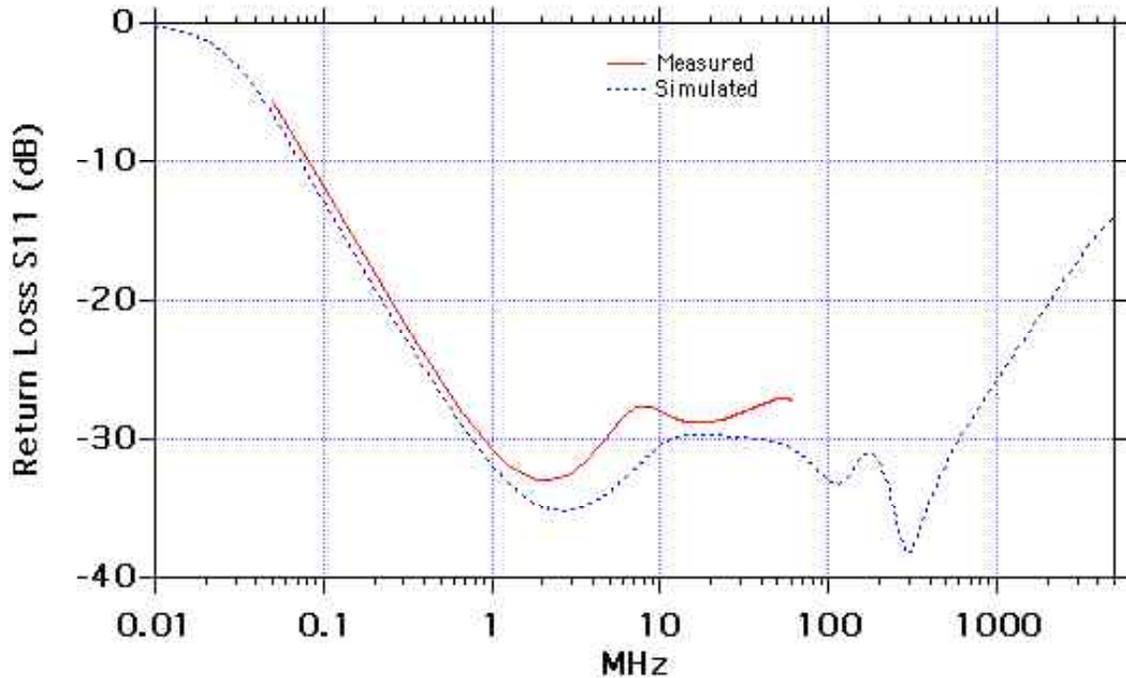
Bill of Materials **Rev. 0, 5-3-08**

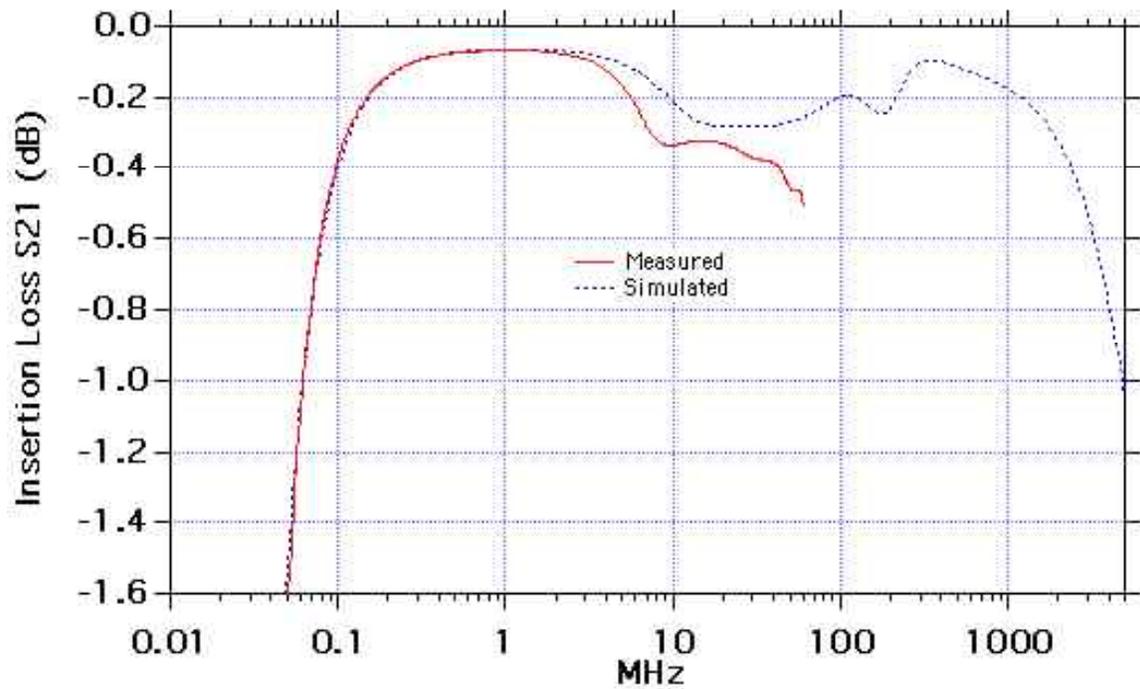
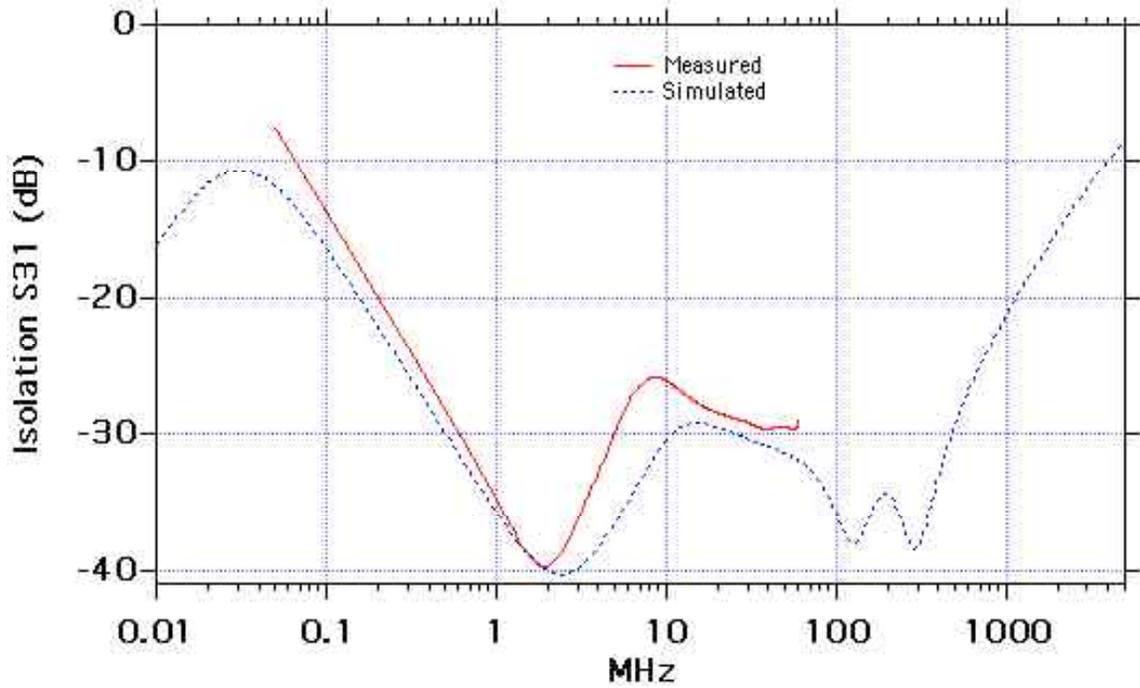
Ref	Quan	Value	Mfg., P/N
C1, C2	2	27nF, 100 V, 5%, 0805, X7R	
C3	1	1pF, 100 V, 5%, 0805, C0G	
C4	1	10pF, 100 V, 5%, 0805, C0G	
C5	1	10nF, 100 V, 5%, 0805, X7R	
L1	1	330nH, 10%, FERRITE SHIELDED SMT	API Delevan S1008R-331K
L2	1	910nH, 10%, FERRITE SHIELDED SMT	API Delevan S1008R-911K
L3	1	18uH, 10%, FERRITE MOLDED SHIELDED	API Delevan 1641R-183K
L4	1	470uH, 15%, POWER INDUCTOR	API Delevan 2474R-33L
R1, R2, R3, R5, R6, R7	6	1.50K, 1%, 0805	
R4	1	5.11K, 1%, 0805	
J1, J2	2	SMA jack, end launch	
J3	1	BNC jack, right angle	TYCO/AMP 227677-1



Performance

The bias tee was characterized on my N2PK VNA over its available frequency range of 50 kHz to 60 MHz. Software was VN4Win, V1.3b. I plan to retest it on an HP 8753B at work to check higher frequencies. Graphs below show performance with 50 ohm terminations at all three ports with simulation curves overlaid for model validation. Toward the high end, S11, S21, and S31 are all a bit worse than the model but I'd say the model is a very useful predictor within our knowledge of component and layout parasitics. Overall, this bias tee meets my basic requirements over this range.

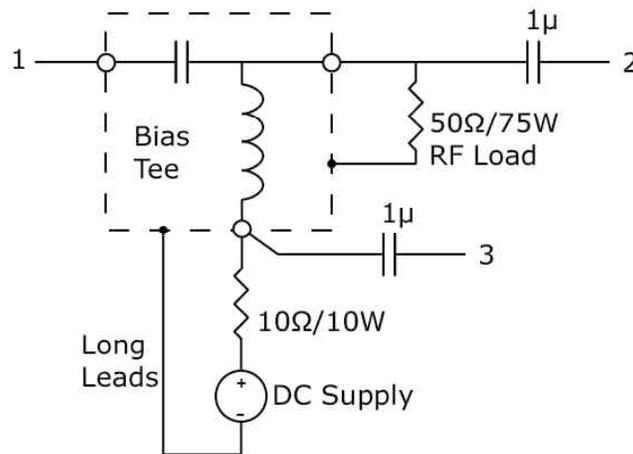




Adding a 1 μF tantalum capacitor at the DC port improved S31 by 35 dB at all observed frequencies. This is consistent with simulation.

DC Saturation Test

DC saturation was evaluated by applying current from a power supply to the DC port while measuring S21 and S31 per the diagram below. The challenge was to dissipate the DC power in a load external to the VNA. I ended up using a 50 ohm dummy load, so port 2 is double-terminated during testing. This makes the absolute measurements different from the normally-terminated cases, but still usable for relative testing where the only variable is DC current.



Up to 250 mA (maximum rated current for L3), differences were negligible: 0.16 dB for S31, and within instrument uncertainty for S21. So it appears these inductors were not exhibiting significant saturation at this current.

Going Lower in Frequency

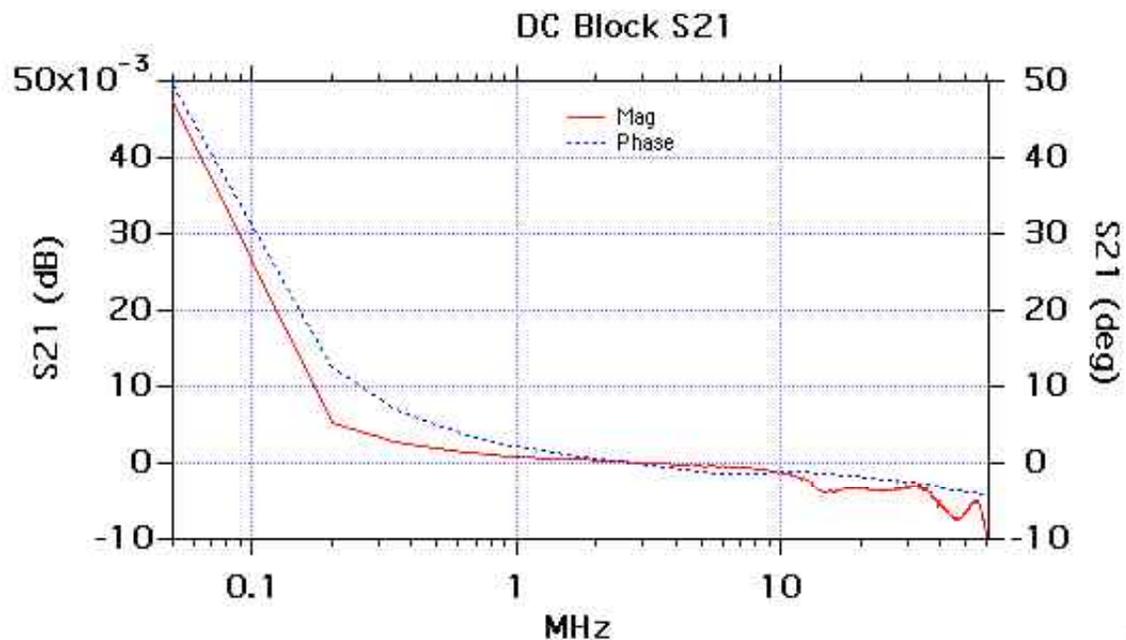
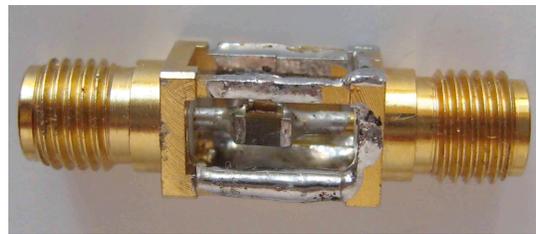
Obtaining a lower cutoff frequency is straightforward. Increasing the coupling capacitor proportionally lowers cutoff for S11 and S21 but has no effect on S31. Increasing the large inductor L4 lower the cutoff for S31 but does not affect S11 or S21. Capacitor high-frequency characteristics may become problematic, especially ESL. Using two or more smaller parts (of equal value) in parallel is a good approach.

The biggest challenge may be practical in that the inductor will become bulky, at least if you want high DC current capability. Picosecond Pulse Labs supplies these large inductors as separate, external components or sub-circuits intended to reside outside the compact RF-shielded bias tee housing, which makes sense because it's only working with audio frequencies. RC damping is still applicable, especially if pulse fidelity is important.

An Accessory: Connectorized DC Block

Another test accessory that's useful with a bias tee is a connectorized DC block. I fabricated mine from a pair of SMA thru-hole PCB jacks. The center pin on one jack is shortened 0.050 inches, then the two connectors are soldered together as shown. A strip

of thin brass sheet is bent around two sides, crimped to hold the assembly together, and then soldered. Capacitors are a 1.0 μF ceramic 1206 SMT in parallel with a 100 pF 0805. The latter may not be necessary. Loss through the HF region is under 0.01 dB.



Bibliography

Andrews, James R., *Broadband Coaxial Bias Tees*, Picosecond Pulse Labs Application Note 1E. <http://www.picosecond.com/objects/AN-01e.pdf>

Baylis, Charles, et. al., *Design of Bias Tees for a Pulsed-bias, Pulsed-RF Test System Using Accurate Component Models*. **Microwave Journal**, Oct., 2006.

SHF Communications Technologies AG, *Impact of Bias Tees on Communication Signals*, Application Note AN-BT65-1.

http://www.shf.de/en/communication/downloads/application_notes/getfile/21/269/

Makers of Broadband Bias Tees

Aeroflex Inmet, http://www.inmetcorp.com/imprdBias_Tees.htm

Marki Microwave, <http://www.markimicrowave.com/>

Picosecond Pulse Labs, <http://www.picosecond.com/>
SHF Communications Technologies, <http://www.shf.de>